UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,939	12/13/2001	Takashi Norimatsu	PW 0277026 H7608US	2669

7590 02/14/2006

Pillsbury Winthrop LLP
Intellectual Property Group
725 South Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406

EXAMINER	
CHANKONG, DOHM	
ART UNIT	**PAPER NUMBER**
2152	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,939	NORIMATSU ET AL.	
	Examiner	Art Unit	
	Dohm Chankong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1> This action is in response to Applicant's amendment and remarks, filed 11.9.2005. Claims 1-21 are presented for further examination.

2> This is a final rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3> Claims 1-6, 12-15, and 19-21 are rejected rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. In particular, independent claims 1, 4, 12 and 19 are rejected for lacking proper antecedent basis: "the same relative timings" and "the relative input timings".

Response to Arguments

4> Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendment.

5> With respect to claim 8, Applicant argues that Turner's shift register is not directed towards input timings. However, based on the construction of the rejection, Sasaki was the

primary reference, disclosing a time register dealing specifically with input timings [column 11 «lines 25-42»] but did not expressly disclose a shift register. Turner was meant to teach that Sassaki's time register may be implemented as a shift register, thus allowing for shift timings in Sasaki's register.

Contrary to the previous characterizations of Sasaki [Applicant's arguments, ¶ 3], Sasaki does indeed disclose utilizing bits as a means to keep track of input timings [column 7 «lines 57-60»]. Bits comprise bytes, and thus by implication, Sasaki discloses bits within his invention in dealing with timing of the input data. Furthermore, a register is well known in the art as being a memory for storing information in byte form. Thus, Sasaki's time register, also by implication, discloses utilizing bits to store timing information.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6> Claims 1-7, 10-12, and 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki, U.S. Patent No. 6.248.945, in view of Mohrbacher, U.S Patent No. 5.902.949.

7> Mohrbacher was cited by the Office in the previous office action, filed 6.6.2005.

8> In regards to claim 1, Sasaki discloses a communication method that is executed by a transmission unit [2701-2703] and a reception unit [2701-2703], comprising:

- packetizing sporadically input data to accompany timing information representing respective input timings of the input data (col. 15 ll. 18-30, col. 25 ll. 59-63, col. 26 ll. 1-39, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7));
- transmitting packetized input data accompanying the timing information from the transmission unit ((col. 15 ll. 18-30, col. 25 ll. 59-63, col. 26 ll. 1-39, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7);
- receiving the packetized input data accompanying the time timing information by the reception unit(abstract, col. 8 ll. 32-35,60-63); and
- outputting the packetized input data as output data timings based on the timing information from the reception unit, wherein consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data (col. 8 ll. 60-63, col. 19 l. 51 to col. 20 l.3).

Sasaki does not expressly disclose that said timing information is represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data.

9> It should be noted that Sasaki discloses: ""The time data to be added to the MIDI data is assumed having 4 bytes representing a time, for example, with a unit of a millisecond" [column 7 «lines 57-60»] as well as a time register to keep track of input timings for the sound information [column 11 «lines 25-42»]. In the same field of invention, Mohrbacher

discloses said timing information being represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data [column 53 «line 34» to column 54 «line 32»].

Mohrbacher utilizes the input timing information to signify the when each note must be played relative to other notes within the composition, hence, a "relative time stamp". As seen in the table, Mohrbacher discloses a time stamp represented by a series of bits. It is well known in the art to use "1" or a "0" within a byte structure to convey information. For example, Mohrbacher utilizes the presence of a "1" to signify the length of a note [column 12 «lines 35-44»].

It would have been obvious to one of ordinary skill in the art to implement Sasaki's timing information as a series of bits as taught by Mohrbacher. This functionality is implied by Sasaki's use of a byte structure and a time register for maintaining input timings for the sound data. Thus, Mohrbacher simply teaches what is already implied by Sasaki's system.

10> As to claim 4, as it does not teach or further define over the previously claimed limitations, it is similarly rejected for at least the same reasons set forth for claim 1.

11> In regards to claims 7 and 16, Sasaki discloses transmission unit [2701-2703] (col. 5 ll. 63-67, col. 10 ll. 11-15) for use in a communication system performing packet communications, comprising:

- input device[130] for inputting sporadically input data (col. 11. ll. 44-45, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7)

- a buffer memory [103] for accumulating the sporadically input data, wherein the buffer memory is periodically initialized every prescribed time [predetermined time lapses] (col. 15 ll. 18-30, col. 25 ll. 59-63, col. 26 ll. 1-39, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7);
- a timing data register [102/104] for storing timing data representing input timings of the sporadically input data(col. 15 ll. 18-30, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7); and

a controller [101] for periodically checking store content of the timing data register at every prescribed time, wherein the controller performs packetizing of the sporadically input data stored in the buffer memory, and the packetized input data accompanying the timing data read from the timing data register are subjected to transmission (col. 11 ll. 52-57, col. 15 ll. 34-37, col. 25 ll. 14-30, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7).

Sasaki does not expressly disclose that said timing information is represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data. However, see rejection of claim 1 for reference teaching and motivation with Mohrbacher.

12> In regards to claim 12 and 19, Sasaki discloses a reception unit [2701-2703] for use in a communication system performing packet communications, comprising:

- a receiver [107] for receiving packetized input data corresponding to sporadically input data from a transmission unit [2701-2703], together with timing data [e.g. timestamp]representing their input timings ((col. 15 ll. 18-30, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7)),

- a buffer memory [103] for accumulating the packetized input data received by the receiver (col. 15 ll. 18-30, col. 25 ll. 59-63, col. 26 ll. 1-39, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7);
- a timing data register [102/104] for storing the timing data received by the receiver (col. 15 ll. 18-30, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7); and
- a controller [101] for outputting, as output data, the packetized input data read from the buffer memory at timings based on the time timing data such that consecutive pieces of said output data are outputted at the same relative timings as the relative input timings of the corresponding input data (col. 11 ll. 52-57, col. 15 ll. 34-37, col. 19 l. 51 to col. 20 l.3, col. 25 ll. 14-30, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7)

Sasaki does not expressly disclose that said timing information is represented by a series of bits, wherein, within a given time interval, a bit value of "1" indicates an input timing for a specific piece of input data. However, see rejection of claim 1 for reference teaching and motivation with Mohrbacher.

13> In regards to claims 2, 5,10, 14, 17 and 20 Sasaki discloses wherein the sporadically input data correspond to MIDI data[114,130] that are produced and input to the transmission unit(input via [130]) in a sporadic manner(col. 5 ll. 35- 38 col. 15 ll. 18-30).

14> In regards to claims 3, 6, 11, 15, 18, and 21 are Sasaki discloses wherein the transmission unit [2701-2703] transmits the packetized input data accompanying the timing information to the reception unit [2701-2703] via a network (col. 31 ll. 20-29, col. 5 ll. 38-39).

15> Claims 8-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki and Mohrbacher, in further view of Turner, U.S Patent No. 5.339.311.

16> In regards to claim 8, Sasaki discloses the transmission unit according to claim 7,

Sasaki does disclose a time register storing input timing data [column 11 «lines 32-42» whereby the register is incremented in response to a packet timing. Sasaki does not expressly disclose wherein the prescribed time corresponds to a packet timing that occurs by a prescribed number of shift timings corresponding to bits of the timing data respectively.

Turner discloses wherein the prescribed time corresponds to a packet timing that occurs by a prescribed number of shift timings corresponding to said bits of the timing data respectively (col. 4 ll. 12-col. 5 ll. 4).

It would be obvious to one of ordinary skill in the art at the time of the invention to modify Sasaki by having packet timing that occurs by a prescribed number of shift timings corresponding to bits, as taught by Turner (col. 2 ll. 11-47). Turner's shift registers would be useful in furthering Sasaki's functionality of playing the input data at the correct sequence: "When the reception of the performance data from each of the apparatuses 1302 to 1304 is completed, the CPU 101 of the apparatus 1301 sorts event data (in this case, MIDI data) in the order of their earlier performance timings specified by time data added to the event data" [see Sasaki, column 19 «lines 51-55»].

Thus, such functionality was already suggested by Sasaki's disclosure of incrementing the time register.

17> In regards to claim 9 and 13, Sasaki discloses the transmission/reception unit [2701-2703] according to claim 7, wherein the timing data register [102/104] stores the timing data (col. 15 ll. 18-30, col. 31 ll. 20-29, col. 31 ll. 50 -col. 32 ll. 7)

Sasaki does not disclose wherein the timing data register is a shift register for storing the timing data having a prescribed number of bits every prescribed time corresponding to packet timing.

Turner discloses wherein a timing data register [46] is a shift register for storing the timing data (col. 4 ll. 12-20) having a prescribed number of bits every prescribed time corresponding to a packet timing (col. 4 ll. 20-65]).

It would be obvious to one of ordinary skill in the art at the time of the invention to modify Sasaki by having a shift register, as taught by Turner in order to determine the sequence in which packets thereby by controlling the transmission of data packets (col. 2 ll. 11-47).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dohm Chankong whose telephone number is 571.272.3942. The examiner can normally be reached on Monday-Thursday [7:00 AM to 5:00 PM].

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571.272.3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER

DC